REMARKS

Applicants respectfully traverse and request reconsideration.

Claim 24 stands rejected under 35 U.S.C. § 112, 1st paragraph, as allegedly failing to comply with the written description requirement due to the Applicants not having possession of the claimed invention. In particular it is alleged that the data storage device coupled to an I O controller via a second high speed bus is not disclosed or supported by the original specification. Applicants respectfully wish to point out that the subject matter is specifically shown in Figure 1 and described in connection therewith. (See e.g. page 6, 2nd paragraph). For example, the specification notes that a high speed bus 121 and bus 133 are both coupled to the I O controller 130. A hard drive 150 which is a data storage device as known in the art, is coupled via high speed bus 133. In any event, Applicants have amended the claim to indicate that the data storage device is coupled to the I O controller via a different bus.

Claims 18-20 and 22-23 stand rejected under 35 U.S.C. § 13(a) as being unpatentable over the combination of Iachetta, Porterfield, Ajanovic, and Heil. Claim 18 as amended, requires, among other things, that the I O controller is coupled to a high speed bus arbiter via a high speed bus and has a low speed arbiter coupled to a low speed bus wherein the low speed bus arbiter supports a slower bus rate than a high speed arbiter and the I O controlled includes a separate bus coupled to a data storage device. In addition, claim 18 requires a system controller having a first memory channel controller, a second memory channel controller and a high speed bus arbiter. The cited references alone or in combination fail to disclose or teach the claimed subject matter. It is admitted that Iachetta fails to disclose, among other things, an I O controller coupled to a high speed bus arbiter via a high speed bus and it does not disclose that the arbiter is an integrated part of the controller nor does it disclose two separate memory channel controllers.

In addition, Applicants respectfully submit that it fails to show an I O controller with the bus and control configuration as claimed. In addition Porterfield is directed to a method and system for avoiding live lock conditions on a computer bus. Therefore Porterfield describes a mechanism wherein in response to receiving a transaction request from a first bus master, a bus controller transmits a retry command to the first bus master if the bus controller is unable to execute the transaction request. In addition, the system controller of Porterfield is similar to that shown in Iachetta and also does not describe or teach an I O controller as claimed.

Ajanovic is directed to a triple port bus bridge that supports a primary bus and two secondary busses. It is alleged that the bus bridge of Ajanovic is an I O controller. However, it does not appear to provide any I O device control and as such, Applicants respectfully submit that Ajanovic does not teach what is alleged. In addition, Ajanovic has been cited as teaching to ccntralize bus request arbitration with dedicated buffers. Applicants are not claiming such structure. Accordingly, Applicants also submit that the cited teachings do not appear to be relevant to the claimed subject matter. Ajanovic while teaching a triple port bus bridge (not an I O controller) also fails to teach the high speed and low speed arbitration logic that is claimed and no portion of the references are cited as teaching the subject matter. The combination of Iachetta, Porterfield and Ajanovic hence fail to teach the claimed subject matter. If the rejections are maintained, Applicants respectfully request a showing as to the teaching in the cited references of the claimed subject matter of the low speed and high speed arbiter coupled to the specific busses and where a separate bus is coupled to the data storage device as claimed. Heil also admittedly fails to teach an I O controller with the claimed low speed and high speed arbitration logic and bus as claimed. Accordingly, the claim is a condition for allowance.

The dependent claims add additional novel and non-obvious subject matter.

Claims 22 and 23 have been cancelled without prejudice.

As to new claim 25, Applicants respectfully submit that the cited portions of the references do not teach or suggest unified memory coupled to the structure set forth in claim 18 for the relevant reasons above and as such Applicants respectfully submit that the claim is in condition for allowance.

Accordingly, Applicants respectfully submit that the claims are now in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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